ABSTRACT OF THE INVENTION

A reliable, inexpensive "back side" thinning process and apparatus therefor, capable of globally thinning an integrated circuit die to a target thickness of 10 microns, and maintaining a yield of at least 80%, for chip repair and/or failure analysis of the packaged die. The flip-chip packaged die is exposed at its backside and mounted on a lapping machine with the backside exposed. The thickness of the die is measured at at least five locations on the die. The lapping machine grinds the exposed surface of the die to a thickness somewhat greater than the target thickness. The exposed surface of the die is polished. The thickness of the die is again measured optically with high accuracy. Based on the thickness data collected, appropriate machine operating parameters for further grinding and polishing of the exposed surface are determined. Further grinding and polishing are performed. These steps are repeated until the target thickness is reached.